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AN EFFICIENT CORDIC USING FACTOR SHARING METHOD IN DIGITAL IMAGE PROESSING

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ABSTRACT

CORDIC (Co-ordinate Rotational Digital Computer) plays a major role in shift and add operation in trigonometric, hyperbolic function in shifting and adding cosine, sine, tangent function. In this paper CORDIC is used in Discrete cosine transform as a multiplier unit. DCT is modified using column bypass and row bypass technique to increase the speed and to reduce the delay with less complexity for that purpose a technique called factor sharing method is proposed in CORDIC architecture which is implemented using video compression for real time application. CORDIC using DCT is done using MODELSIM6.4a by taking video compression as a input, where the video is been converted into text file using the MATLAB software.

Keywords: CORDIC, factor sharing, video compression.

1. INTRODUCTION

The Introduction gives a clear idea of CORDIC, video compression, discrete cosine transform, algorithm and its uses in real time application.

1.1 CORDIC

Coordinate Rotation Digital Computer Invented in late 1950's Based on the reflection that, if you rotate a unit-length vector (1,0) by an angle y its new end-point will be at (cos y, sin y).CORDIC algorithm and its improvement has raised higher when it is been survived deeply in almost all fields. When noticed in algorithm design the CORDIC has given high importance, which has been recognised in giving high performance and low-cost hardware. In aiming high output performance the best architectures are parallel and pipeline design. One of the best achieved methods was reducing the redundancy in the circuit, which reduce power deliberately. When the redundant values are eliminated automatically the performance in the circuit increases with also increases in speed. By using Taylor series the CORDIC is used in initially aimed in designing scale-free co-ordinate to obtain Scaling-free CORDIC. To remove the scaling factor Taylor series is used as a disposing factor [1]. It Can evaluate efficiently all functions of k iterations require for k-bits accuracy. CORDIC algorithm is used in much architecture for hardware purpose. There are three different approaches used in hardware architectures they are, sequential approach which is nothing but an arrangement of folded architectures with respective to time, and then comes the parallel approach in which the structure is obtained using unfolded architecture using space or grouping two functions. A sequential CORDIC attains one iteration per clock cycle and consists of three n-bit adders or subtractors in the architecture, two sign spreading shifters, a look-up Table (LUT) for the step angle coefficients and a finite state machine.[3]. The parallel CORDIC is very much similar to an array multiplier structure which consists of rows obtaining adders or subtractors. Combination of both parallel and sequential architecture of CORDIC is designed on a sequential structure where the logic for numerous successive iterations is constructed and is performed on single clock cycle. Arithmetic addition is calculated using the CORDIC algorithm, the efficiency of the hardware implementation of the algorithm depends totally on what type of adders are used. Two methods are used in sequential CORDIC operation they are Bit-serial and binary adders and in cascaded CORDIC designs all types of adders are performed such adders are bit-serial adders, carry-save adders, binary adders, redundant adders, combinations of binary adders and redundant adders.

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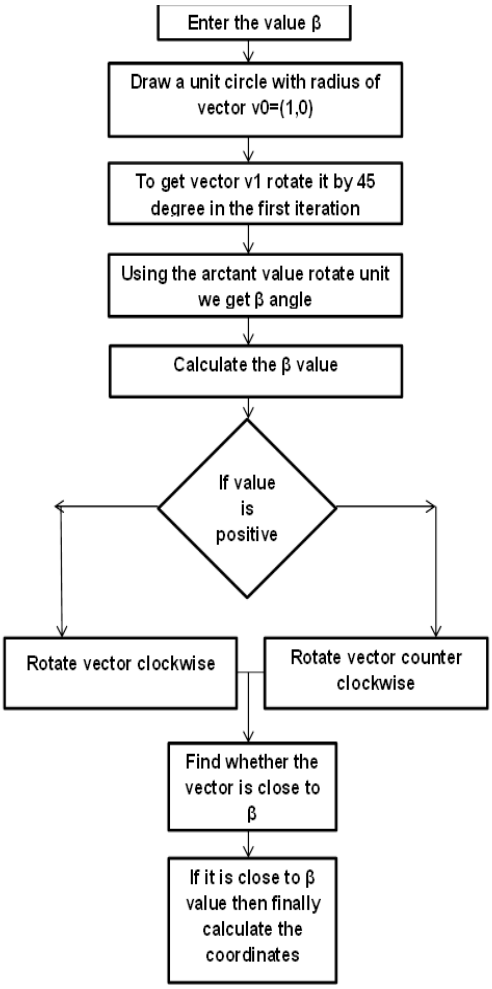

Figure-1. Flow diagram for CORDIC operation.

When considering the combination of sequential approach and bit-serial adders will achieve less area but the major drawback is the results obtained will be very slow, when observing the parallel approach and redundant adders the outcome is fast but observes more area. CORDIC is calculated as shown in the flowchart below, this description demonstrates how to use CORDIC in rotation mode to calculate sine and cosine of an angle, and accepts the desired angle is given in radians and represented in a fixed point setup. To define the sine or cosine the y or x coordinate of an angleβ is determined using a point on the unit circle consistent to the desired angle must be found. By means of CORDIC, we should start with the vector vo =(1,0). In the first repetition, this vector would be rotated 45° counter clockwise to get the vector v1. Successive iterations will rotate the vector in one or the other way by size decreasing steps, until the desired angle has been attained. Step i size is arctant (1/(2i−1)) for i = 1, 2, 3, ….is shown below, The flowchart of the CORDIC operation is calculated using the vector and rotator mode. The values are computed according to the steps given in the Figure-1.

1.2 Discrete cosine transform

DCT is mainly used in compressing images and videos using degradation technique which is essentially used in digital image processing. Computer which are widely used for storing purpose in large scale level helps in storing huge amount of data transmission, thus storing large data's has become an essential factor in today's scenario. Image compression is reducing the size in bytes of a graphics file without degrading the quality of the image to an improper level. When the folder size decreases it permits more images to be stored in a given amount of memory space. [7]It also decreases the time required for images to be led over the Internet or downloaded from Web pages. JPEG and JPEG 2000 are two vital systems used for image compression. DCT (DISCRETE COSINE TRANSFORM) uses JPEG image compression standards. The discrete cosine transform is a firm transform. It is a widely used in robust method for image compression. It has outstanding compaction for extremely associated data. DCT has secured basis images DCT gives good compromise between information packing ability and computational difficulty. Image compression is very significant for well-organized transmission and storing of images.

The Digital image processing (DIP) is used in computer algorithms to perform image processing on digital images. The basic procedure achieved by a simple digital camera is, to transform the light energy to electrical energy, then the energy is transformed to digital format and a compression algorithm is used to reduce memory necessity for storageof the image. [9]This compression algorithm is frequently called for capturing and storageof the images. This leads us to progress of an efficient compression design which will give the related outcomes as that of the existing algorithms with low power consumption. Compressing an image is valuable as it supports in decrease of the practice of exclusive properties, such as memory, or the transmission bandwidth necessary. But on the downside, compression methods result in distortion and also additional computational resources are required for compression and decompression of the remedial image data. The DCT mainly used for compressing image and video. Thus mostly used in digital signal processing.

1.3 Video compression

Video compression technologies facing lot of challenges in current days, they are about reducing and removing redundant video data so that a digital video folder can be efficiently sent over a network and stored on computer disks. With strong compression systems, a trivial reduction in file size can be attained with few or no adverse effect on the visual quality. The video quality can be exaggerated if the file size is further lowered by raising

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the compression level for a given compression technique. [10] Most network video vendors currently use standard compression methods. Standards are important in authorizing compatibility and interoperability. They are predominantly relevant to video compression since video may be used for dissimilar resolves and, in some video observation applications, desires to be accessible many years from the recording date. By organising standards, end users are able to pick and choose from unlike sellers, rather than be tangled to one dealer when designing a video surveillance system. Axis uses three different video compression standards. They are some video standards which are used widely today some are Motion JPEG, MPEG-4and H.264. H.264 is the latest and most efficient video compression standard.H.264 plays a major role nowadays. [15]

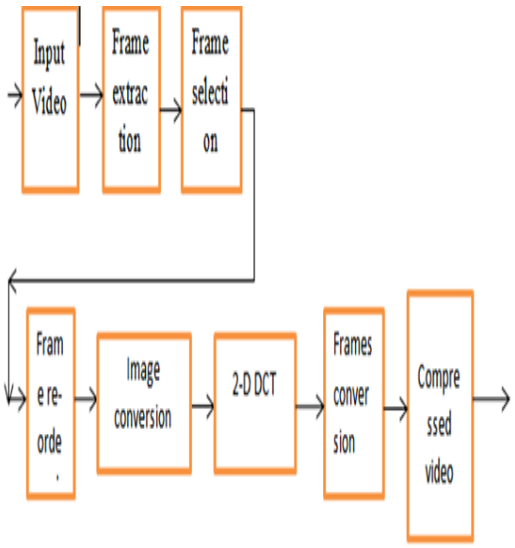

Figure-2. Block diagram of video compression.

In the above block diagram a input video is given which is extracted using frame extraction then the video is converted into 120 frames/sec. From the 120 frames required, frame can be selected using frame selection and frame re-ordered. Then the frame is converted into image used in DCT and finally the video is compressed. This is the basic operation of a video compressing in digital image processing.

2. EXISTING METHODOLOGY

In the existing work the CORDIC algorithm is proposed using Taylor series. Algorithm for vectoring and rotating CORDIC is designed using iteration or the precomputing values. CORDIC is used for shift and add operation for trigonometric function it acts as a multiplying unit. Discrete cosine transformation is used in compressing image and video frames. In this paper video is taken as a input to the DCT. It works in two mode of operation in which it plays the role of multiplier in both vector and rotation mode. It uses pre and post processing circuit using the precomputation logic. The precomputation logic is used for calculating the values earlier. Huge amount of values can be computed and while processing the simulation, the CORDIC instinctively gets shifted using the angles which are previously precomputed. Consequently makes the operation fast and easy for calculating. The simulation result for the precomputing logic is simulated using MODELSIM.[5]

3. PROPOSED WORK

The CORDIC is used as a multiplying unit in DCT, where the DCT is modified using column bypass and row bypass technique to enhance the speed in the operation. The values are assigned simultaneously in row and column. Once the column is achieved the row values are calculated with respective to 0's and 1's.Modified CORDIC uses the factor sharing method. In which the co-efficient are taken common and multiplied, by which the co-efficient are reduced and function fast. The proposed method, by expanding the coefficients matrix at the bit level, the factor sharing method first shares the same factor in each coefficient. When we take video compression the difference between first frame and second frame are similar only some changes occur so the part remaining same is again not calculated in that place, therefore in that place factor sharing method is used. Therefore give increase in speed andobviously consumes less power and DCT helps in reducing complexity in the architecture. For the purpose of real time application it is used in digital image processing using video compression.

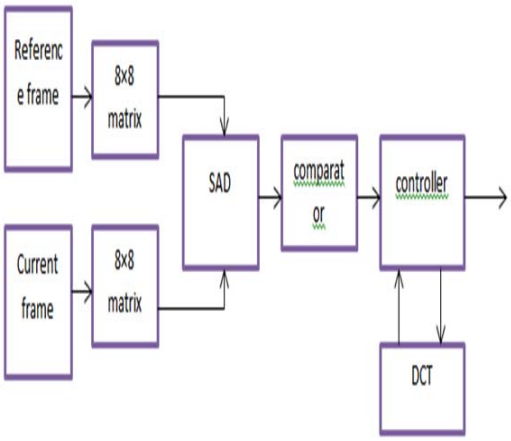

Figure-3. Proposed block diagram of factor sharing method.

In the above block diagram reference frame and current frame are evaluated by using 8×8 matrix and from the matrix sum of absolute difference is calculated and compared the same values are kept with determining their co-efficient since it remains constant, then implemented in

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DCT and used for compression of video in real time application.

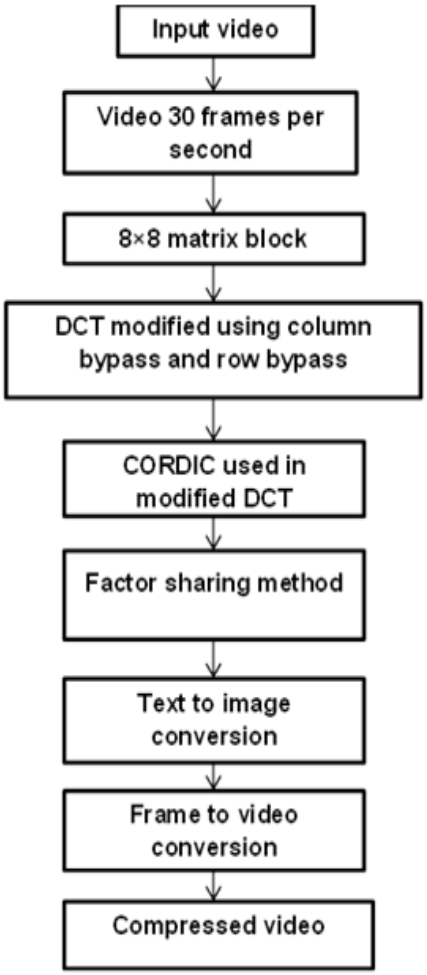

Figure-4. Flow chart for the proposed work.

4. EXPERIMENTAL RESULTS

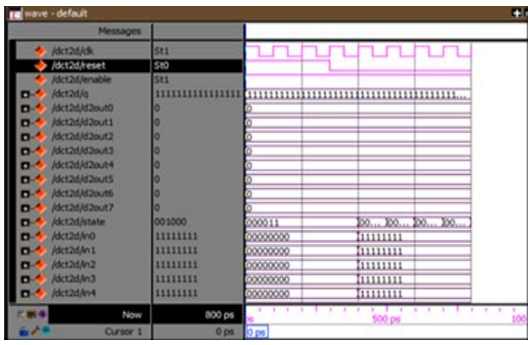

Figure-5. Simulated output for existing CORDIC.

The above Figure explains the output of existing CORDIC in which the input is clk, rst, enable, and q is the output for 8×8 matrix.

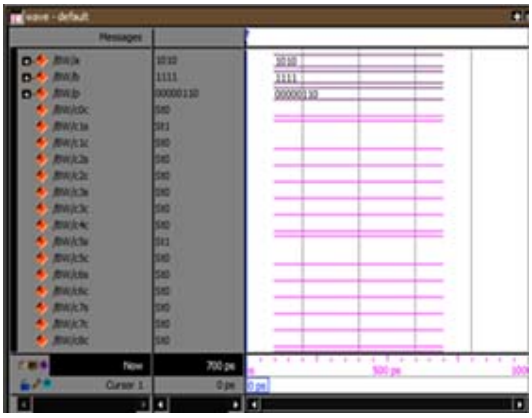

Figure-6. Simulation result of modified DCT.

Figure-6 shows the simulated output of modified DCT with inputs a, b and output p. consider the values given for a=1010 and b=111 the output obtained is p=00000110. Without any values to be given at each time the values are obtained sequentially.

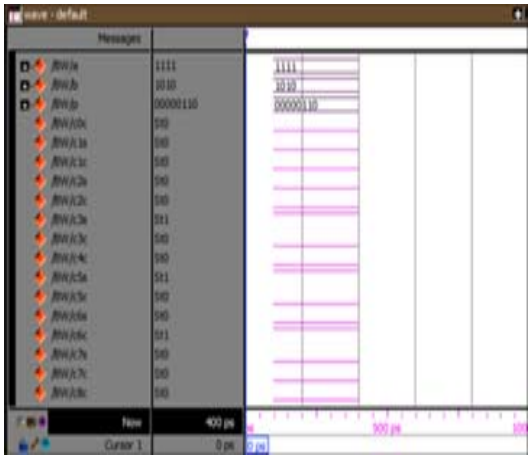

Figure-7. Simulation result of factor sharing method.

Figure-7 is the output obtained from factor sharing method, in which the Input is a,band the output is p

5. PERFORMANCE ANALYSIS

The power consumption, delay, total number of logic elements, total number of register. The result is analysed for factor sharing method.

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Table-1.

Parameters	Existing work	Proposed work
Power consumped	134.11mW	78.06mW
Delay	11.24ns	10.65ns
Total number of logic elements	11.464	6.562
Total number of register	4259	1711

6. CONCLUSIONS

The Factor Sharing Method in CORDIC is used in reducing the power consumption and also in increasing the speed of the operation, by reducing the co-efficient to zero. Digital image compression is used for implementing CORDIC in real time applications. The output is analysed and compared using quartus-11 software. 41.79% of power has been reduced from the existing work using factor sharing method. Video compression is implemented in MATLAB software and taken as a input to the modified CORDIC in DCT. For which MODELSIM 6.4a is used. Results are analysed using QUARTUS-11 software. Factor sharing method gives high performance and high quality to the video therefore it can be implemented in high efficiency video codec, which gives importance in real time applications.

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