VOL. 10, NO. 10, JUNE 2015 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

DESIGN AND IMPLEMENTATION OF PLL BASED FREQUENCY SYNTHESIZER WITH SELF CORRECTING DCO

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ABSTRACT

A phase-locked loop (PLL) is widely employed in wire line and wireless communication systems. The poor device matching and leakage current vary the common-mode voltage of a ring-based voltage-controlled oscillator (DCO) wide frequency range. It may limit the oscillation frequency range of a DCO and causes a DCO not to oscillate in a worst case. To realize a wide-range PLL, the divider following a DCO should operate between the highest and lowest frequencies. When a PLL works at a higher frequency which the static circuits cannot operate, dynamic circuits are needed. A true-single-phase-clocking (TSPC) divider is widely used to realize a prescaler for this PLL. A TSPC prescaler must work over a wide frequency range to cover the process and temperature variations. For a TSPC prescaler, the undesired leakage currents may limit its frequency range or alter the original states of the floating nodes to have a malfunction. The leakage current and current mismatch in a charge pump (CP) will degrade the reference spur and jitter significantly. In the previous method to overcome the above problems, a self-healing divide-by-4/5 prescaler and a self-healing DCO is used. A time-to digital converter (TDC) and a 4-bit encoder are used to quantize the phase error and digitally calibrate the CP. In the existing method the key parameter is to be changed is the modulus value of the prescaler. By changing the value of the prescaler the PLL frequency range will be extended.

Keywords: true-single-phase-clocking (TSPC), digitally controlled oscillator (DCO).

I. INTRODUCTION

Phase-locked loops (PLL) have become essential components in wireless communication systems. They are used as frequency synthesizers with precise and convenient digital control in both traditional electronics, such as televisions and AM/FM radios, and modern consumer products among which cellular mobile phone is a striking example. IC fabrication technology advances have made monolithic integration possible. More and more electronic devices can be put on the same chip to reduce the number of external components and then the costs. Therefore, on a single chip we can accomplish many functions for which we might need to make several chips work together a few years ago. A monolithic wide-band PLL is of great interests to wireless communication applications due to both its low cost and convenience to switch between different communication standards. The focus of this work is to implement a monolithic wide-band PLL using as few as possible building blocks and also as simple as possible structure.

2. DESIGN SPECIFICATIONS

The desired wide band PLL should be able to cover different standards with large frequencies. Our design will be based on a wide-band DCO shows an output frequency range of 1.14-2.47GHz, we will try to design the PLL to cover all digital cell phone standards including TDMA IS-54/IS-136, CDMA, GSM, DC1800/DC1900, and PDC. The design of PLL based frequency synthesizer with self correcting DCO includes Delay detector, Signal Shaping Circuit, DDS synthesizer, DCO corrector, Frequency divider.

3. DELAY DETECTOR

The first stage of the ADPLL is the phase detector as it was for the PLL. In the case of the ADPLL the phase detector consists of either an EXOR gate or an edge triggered phase detector. The EXOR type is simply an EXOR logic gate. This type of detector locks itself 90 degree behind the phase of the input signal. Two drawbacks to this type of phase detector is that it has a phase error limit of + or - 90 degrees and it is not sensitive to edges in the signal but rather the flat section. Below is an example of the "locked" state. The big advantage of Delay detector is it consists of only one logic gate.

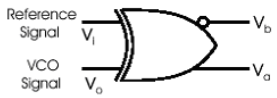

Figure-1. Representation of LOGIC gate (Delay Detector).

4. SIGNAL SHAPING CIRCUIT

The next stage of the loop is the signal shaping circuit (loop filter). The loop filter that always works with the EXOR and the edge triggered phase detectors is the K counter. This loop filter contains two separate counters

both of which are counting upward. The UP/DN bit determines which counter is running at any moment. The K clock is M*F0 where M is a large integer (8, 16, 32) of the reference signal F0. The carry and borrow outputs are the most significant bits of the counters and are only high when the contents of a particular counter are greater than K/2. These values are used to control the DCO (digitally controlled oscillator). The counters are reset when the contents reach a value of K - 1.

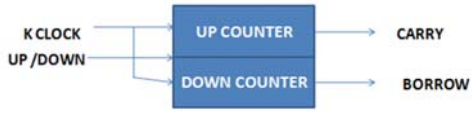

Figure-2. Block diagram of Signal Shaping Circuit.

5. DDS SYNTHESIZER AND SELF CORRECTING DCO

Direct Digital Synthesizer is a type of frequency synthesizer used for creating arbitrary waveforms from single, fixed-frequency reference clock. Applications of DDS include: signal generation, local oscillators in communication systems, generators, mixers, modulators and as part of a digital phase-locked loop. A basic Direct Digital Synthesizer consists of a frequency reference (often a crystal or SAW oscillator), a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC). The reference oscillator provides a stable time base for the system and determines the frequency accuracy of the DDS. It provides the clock to the NCO which produces at its output a discrete-time, quantized version of the desired output waveform (often a sinusoid) whose period is controlled by the digital word contained in the Frequency Control Register. The sampled, digital waveform is converted to an analog waveform by the DAC. The output reconstruction filter rejects the spectral replicas produced by the zero inherent in the analog conversion process.

6. IMPLENTATION RESUTS

The design is scripted as a VHDL file and synthesized using modelsim. Below diagram shows how results of this paper.

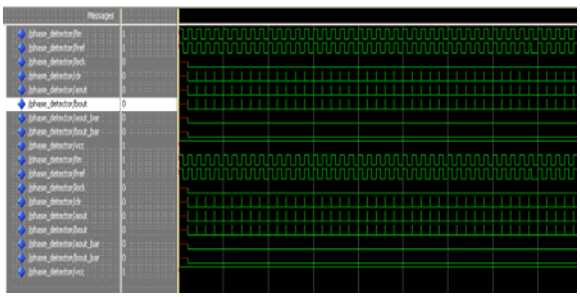

Figure-3. Output wave form of Delay detector when f_{in}=1.

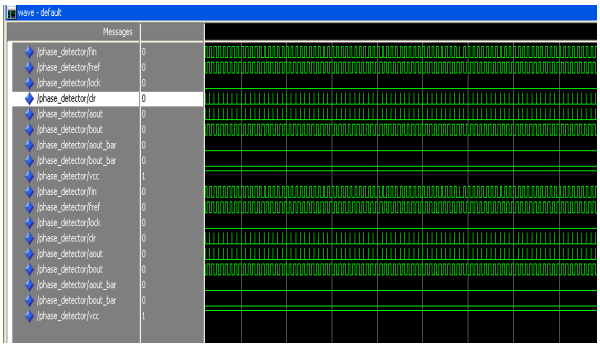

Figure-4. Output wave form of Delay Detector when f_{in} =0.

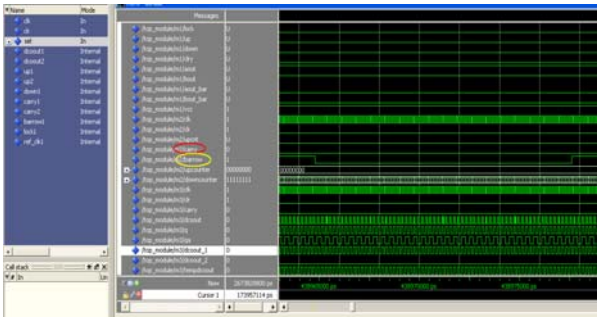

Figure-5. Loop filter output wave form.

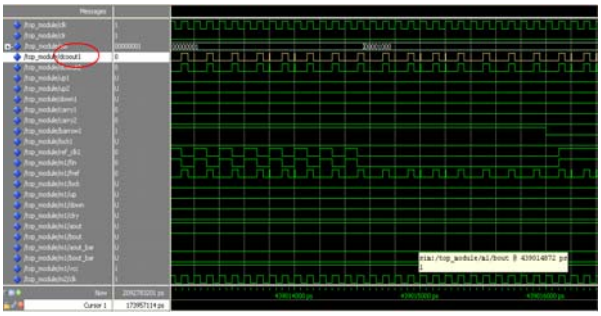

Figure-6. Output wave form of direct digital synthesizer and DCO corrector.

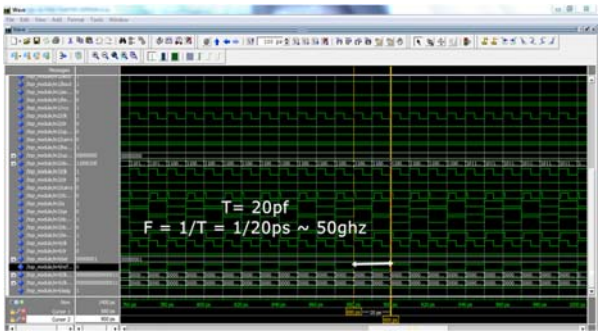

Figure-7. Final output.

7. COMAPARISION TABLE

TYPE OF SYSTEM	DELAY	FREQUENCY
EXISTING SYSTEM	200ps	5GHZ
PROPOSED SYSTEM	20ps	50GHZ

8. CONCLUSION AND FUTURE SCOPE

A digital phase locked loop can have many uses. In spread spectrum, the code or clock synchronization is an important step in the decoding process. If the data bits or clock bits are out of phase then the decoded bits could be decoded incorrectly. Also, if the decoder tries to decode the bits away from the centre of the bits then slight variations could cause the decoder to decode the wrong bit. The loop could also be used to synchronize to a repeatable code. This could be important if the dispreading code needed synchronized to the input.

An interesting research topic to branch off of this paper would be an all digital phase lock loop that locks to analog signals. The loop in this research paper synchronizes only digital type signals. An analog signal could be taken through the analog to digital converter and locked to in the loop before being retranslated through the digital to analog converter back to analog. All of the analog math in the analog phase lock loop could be translated to discrete math and done in an FPGA

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